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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LOKE, STEVEN HO YIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,474	LEHMANN ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6-9,16-20 and 28-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,7,9,16-20,30 and 33-43* is/are rejected.

7)☒ Claim(s) *8,28,29,31 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 8, 28, 29, 31, 32 are objected to because of the following informalities: Claim 8, line 22, claim 28, line 10, claim 31, lines 3, 4, 10, claim 32, lines 9, 15, the phrase "gate oxide electrode" is unclear as to what is it. It is well known in the art that a gate electrode is formed on a gate oxide. It is believed that the phrase should rewrite as "gate electrode". Claim 32, line 7, the phrase "a gate antifuse" is unclear whether it is being referred to "a gate oxide antifuse". Fig. 1 discloses the fuse element [124] is a gate oxide. Appropriate correction is required.

2. Claims 16-20, 30-36 and 38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 16, line 14, the phrase "said counter electrode" is unclear whether it is being referred to "said lower counter electrode".

Claim 33, lines 9-10, the phrase "a gate electrode in contact with the lower fusible insulator portion for interconnecting the lower counter electrode and the common intermediate electrode" is vague and indefinite as to where is the lower counter electrode in the device. The specification (page 16, lines 21-22) discloses the lower gate electrode [125] is the lower counter electrode. Therefore, the phrase should rewrite as "a gate electrode in contact with the lower fusible insulator portion for interconnecting the gate electrode and the common intermediate electrode".

Claim 38, lines 5-7, the phrase "a gate electrode in contact with the fusible insulator portion for interconnecting the lower counter electrode and the common intermediate electrode" is vague and indefinite as to where is the lower counter electrode in the

device. The specification (page 16, lines 21-22) discloses the lower gate electrode [125] is the lower counter electrode. Therefore, the phrase should rewrite as "a gate electrode in contact with the fusible insulator portion for interconnecting the gate electrode and the common intermediate electrode".

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 6, 7, 9, 16-20, 30, 37 and 39-43 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Chang.

In regards to claim 1, Chang shows all the elements of the claimed invention in fig. 2. It is an apparatus, comprising: a semiconductor body [30] having on a surface thereof at least one lower antifuse [36a, 34] and at least one upper antifuse [42a, 48] in vertically stacked relation with both such antifuses sharing a common intermediate electrode [40a] therebetween; the lower antifuse [36a, 34] having a lower counter electrode [34] and a lower fusible insulator portion [36a] defining a lower fuse element of an initial high electrical resistance state interconnecting the lower counter electrode [34] with the common intermediate electrode [40a]; and the upper antifuse [42a, 48] having an upper counter electrode [48] and an upper fusible insulator portion [42a]) defining an upper fuse element of an initial high electrical resistance state interconnecting the upper counter electrode with the common intermediate electrode [40a], wherein the upper antifuse is in the form of a contact antifuse defining a conductive contact [46a]

interposed between the upper counter electrode and the upper fusible insulator portion defining the upper fuse element and interconnecting the upper counter electrode with upper fuse element, the upper fuse element [42a] also being directly interconnected with the common intermediate electrode [40a]; the upper and lower antifuses being arranged to permit their respective selective energizing for corresponding separate or simultaneous activation (col. 6, lines 66-67, col. 8, lines 18-21) to a final low electrical resistance state in both directions between said intermediate electrode and said upper counter electrode and in both directions between said intermediate electrode and said lower electrode (Since all the electrodes and vias are made of metal or electrical conductor, the upper and lower antifuses would have low electrical resistance state in both directions).

In regards to claim 6, Chang further discloses the counter electrode [34] of at least one of the antifuses is interconnected by the corresponding fuse element [36a] to the common intermediate electrode [40a] through at least one electrode extension portion [38a] interposed between said fuse element [36a] and the common intermediate electrode [40a].

In regards to claim 7, Chang further discloses the counter electrode [48] of at least one of the antifuses is interconnected by the corresponding fuse element [42a] to the common intermediate electrode [40a] through at least one electrode extension portion [46a] interposed between said fuse element [42a] and the corresponding counter electrode [48].

In regards to claim 9, Chang further discloses an electrode extension portion [46a] interposed between the upper counter electrode [48] and the upper fusible insulator portion [42a].

In regards to claim 37, Chang shows all the elements of the claimed invention in fig. 2. It is an apparatus, comprising: a semiconductor body [30] having a surface and overlying the surface in vertical relation: an upper contact antifuse [42a, 48] having an upper counter electrode [48] and an upper fusible insulator portion [42a] defining an upper fuse element of initial high electrical resistance; a common intermediate electrode [40a] in direct contact the upper fusible insulator portion of said upper contact antifuse and opposing said upper counter electrode; and a lower contact antifuse [36a, 34] having a lower counter electrode [34] and a lower fusible insulator portion [36a] defining a lower fuse element of initial high electrical resistance and interconnecting the lower counter electrode with the common intermediate electrode; the upper and lower antifuses being arranged to permit their respective selective energizing for corresponding separate or simultaneous activation to a final low electrical resistance state in both directions between said intermediate electrode and said upper counter electrode and in both directions between said intermediate electrode and said lower electrode (Since all the electrodes and vias are made of metal or electrical conductor, the upper and lower antifuses would have low electrical resistance state in both directions).

In regards to claim 39, Chang inherently teaches upper and lower activation circuitry for selectively energizing the upper and lower antifuses separately or simultaneously

because all the memory device would require a decoder circuitry and a programming circuitry to program, address and read the memory elements (antifuses).

In regards to claim 40, Chang shows the upper antifuse is in the form of a direct contact antifuse defining a conductive contact [46a] interposed between the upper counter electrode [48] and the upper fusible insulator portion [42a] defining the upper fuse element and interconnecting the upper counter electrode with upper fuse element.

In regards to claims 16, 41, Chang shows all the elements of the claimed invention in fig. 2. It is an apparatus, comprising: a semiconductor body [30] having on a surface thereof at least one lower antifuse [36a, 34] and at least one upper antifuse [42a, 48] in vertically stacked relation with both such antifuses sharing a common intermediate electrode [40a] therebetween; the lower antifuse [36a, 34] having a lower counter electrode [34] and a lower fusible insulator portion [36a] defining a lower fuse element of an initial high electrical resistance state interconnecting the lower counter electrode [34] with the common intermediate electrode [40a]; and the upper antifuse having an upper counter electrode [48] and an upper fusible insulator portion [42a] defining an upper fuse element of an initial high electrical resistance state interconnecting the upper counter electrode with the common intermediate electrode [40a]; the upper and lower antifuses being arranged to permit their respective selective energizing for corresponding separate or simultaneous activation to a final low electrical resistance state in both directions between said intermediate electrode and said upper counter electrode and in both directions between said intermediate electrode and said lower counter electrode (Since all the electrodes and vias are made of metal or electrical

conductor, the upper and lower antifuses would have low electrical resistance state in both directions); and it inherently further comprising energizable fuse activation circuit means (decoder circuitry and programming circuitry are well known circuitry in memory device to activate the memory cells) defining a lower fuse activation circuit for applying and controlling a selective blow voltage across the lower counter electrode and common intermediate electrode at the lower fuse element for fusibly blowing the lower antifuse to reduce electrical resistance there across to interconnect electrically conductively the lower counter electrode and the common intermediate electrode thereat, and further defining an upper fuse activation circuit for applying and controlling a selective blow voltage across the upper counter electrode and common intermediate electrode at the upper fuse element for fusibly blowing the upper antifuse to reduce electrical resistance there across to interconnect electrically conductively the upper counter electrode and the common intermediate electrode thereat.

In regards to claim 17, Chang inherently further discloses unblown or blown fuse activation state sensing and indicating circuit means (sensing and indicating circuits are well known circuits in memory device to sense and indicate the state of the memory in the memory cells) defining a lower fuse state sensing and indicating circuit for sensing and indicating the unblown or blown fuse activation state of the lower antifuse, and further defining an upper fuse state sensing and indicating circuit for sensing and indicating the unblown or blown fuse activation state of the upper antifuse.

In regards to claim 18, Chang further inherently disclose the fuse activation circuit means are arranged for independently applying and controlling a selective blow voltage

for fusibly blowing the lower antifuse, and for independently applying and controlling a selective blow voltage for fusibly blowing the upper antifuse, to permit their respective selective energizing for corresponding separate fuse activation.

In regards to claim 19, Chang further discloses the fuse activation circuit means are arranged for simultaneously applying and controlling a selective blow voltage for fusibly blowing both the lower antifuse and upper antifuse, to permit their selective energizing for simultaneous fuse activation.

In regards to claim 20, Chang further discloses the lower antifuse [36a] and the upper antifuse [42a] are connected in parallel in fuse activation circuit (col. 5, lines 35-37).

In regards to claim 30, Chang further disclose the upper antifuse is in the form of a contact antifuse defining a conductive contact [46a] interposed between the upper counter electrode and the upper fusible insulator portion defining the upper fuse element and interconnecting the upper counter electrode with upper fuse element, the upper fuse element also being directly interconnected with the common intermediate electrode.

In regards to claim 42, Chang further discloses the upper and lower fuse activation circuits may energize the upper and lower fusible insulator portions separately.

In regards to claim 43, Chang further discloses the upper and lower fuse activation circuits may energize the upper and lower fusible insulator portions simultaneously.

5. Applicant's arguments with respect to claims 1, 6, 7, 9, 16-18, 30, 37 and 39-42 have been considered but are moot in view of the new ground(s) of rejection.

6. Claim 8 would be allowable if rewritten or amended to overcome the objection set forth in this Office action.

7. Claims 28, 31, 32 would be allowable if rewritten to overcome the objection set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. Claim 33 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

9. Claim 38 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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December 10, 2005

StevenLoke
Primary Examiner